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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Hongjiang Song	§	Art Unit:	2631
Serial No.:	09/473,740	§		
Filed:	December 28, 1999	§	Examiner:	Don Nguyen Vo
Title:	Synchronization Detection Architecture for Serial Data Communication	§	Docket No.	ITL.0327US (P8030)

Commissioner for Patents
Washington, D.C. 20231

REPLY TO OFFICE ACTION DATED AUGUST 12, 2002

Dear Sir:

In an Office Action mailed on August 12, 2002, claims 1-8 and 15-20 were rejected under 35 U.S.C. § 102(a) as being anticipated by alleged admitted prior art; and claims 9-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the alleged admitted prior art in view of Banker. These rejections are discussed in the corresponding sections below.

Rejections of Claims 1-7:

The method of claim 1 includes buffering bits to accommodate a difference between a first rate of incoming data and a second rate of outgoing data. The method includes during the buffering, detecting whether at least some of the bits indicate a synchronization field.

In contrast to the limitations of claim 1, the alleged admitted prior art (i.e., the Background section) does not disclose detecting whether some of the bits indicate a synchronization field during the buffering of the bits to accommodate a difference between a first rate of incoming data and a second rate of outgoing data. In this manner, page one of the Background section discusses buffering bits to accommodate the difference between incoming and outgoing rates and subsequently detecting whether some of the bits indicate a

synchronization field. However, the Background section does not disclose detecting the synchronization field during the buffering of the bits.

Thus, for at least this reason, withdrawal of the rejections of claims 1-7 is requested.

Rejections of Claims 8-14:

The repeater of claim 8 includes a data recovery circuit to receive an indication of bits of incoming data from a first serial bus and buffer the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data. The repeater also includes a synchronization detection circuit that is coupled to the data recovery circuit. The synchronization detection circuit detects, while the data recovery circuit is buffering the bits, whether at least some of the bits indicate a synchronization field.

Contrary to the limitations of claim 8, the Background section of the present application does not disclose a synchronization detection circuit to detect whether bits indicate a synchronization field while a data recovery circuit is buffering the bits. In this manner, the Background section discusses this detection of the synchronization field after the buffering.

Thus, for at least this reason, withdrawal of the rejections of claims 8-14 is requested.

Rejections of Claims 15-20:

The system of claim 15 includes a first serial bus, a second serial bus and a repeater. The repeater is coupled to the first and second serial buses to receive an indication of bits of incoming data from the first serial bus and concurrently buffer the bits to accommodate the difference between a first rate of the incoming data and a second rate of outgoing data and detect whether at least some of the bits indicate a synchronization field.

Contrary to the limitations of claim 15, the Background section neither teaches nor suggests a repeater to concurrently buffer bits to accommodate a difference between rates of incoming and outgoing data and detect whether at least some of the bits indicate a synchronization field.

Thus, for at least this reason, withdrawal of the rejections of claims 15-20 is requested.

CONCLUSION

In view of the foregoing, withdrawal of the §§ 102 and 103 rejections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0327US).

Respectfully submitted,

Date: 8/27/02

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